Profile Page

Name	:	Dr Ashish Raman
Designation	:	Associate Professor
Department	:	Electronics and Comm. Engg.
Qualification	:	PhD (VLSI Design/nanoelectronics) M.Tech (Microelectronics and VLSI Design) B.E (Electronics and Communication Engineering)
Address	:	Department of ECE NIT Jalandhar Jalandhar, Punjab - 144011
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Research Interests :

Nanoelectronics
VLSI Design
NanoScale semiconductor Devices
RF Design
AI/ML base Approaches in VLSI Desig
Nanoscale Devices Modeling
Low Power VLSI

Other Profile Links :

Google Scholar Link :

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Personal Web Link :

Ashish Raman Click Here

Journal Publications :

Year	Journal	Publication
2023	INTERNATIONAL JOURNAL OF ELECTRONICS (T&F)	Differential RVCO with low power, low phase noise and wider tuning range for PLL application
2023	Microelectronics Journal	Study of ambipolar and linearity behavior of the misaligned double gate-drain dopant-free Nano-TFET: Design and performance enhancement
2023	IEEE Transactions on Nanotechnology	Design and Analytical Assessment of Non-Ideal Ion-Sensitive ?-MIS-(AlGa) 2 O 3 /Ga 2 O 3 High Electron Mobility Transistor

2023	Journal of Electronic Materials, Springer	Noise Distortion Analysis of the Designed Heterodielectric Dual-Material Gate Dopingless Nanowire FET
2022	Transactions on Electrical and Electronic Materials, Springer	Design and Investigation of Dual Dielectric Recessed-Gate AlGaN/GaN HEMT as Gas sensor Application
2022	IETE Journal of Research	Demonstration of Temperature-Dependent Analysis of GAA–?-(AlGa)2O3/Ga2O3 High Electron Mobility Transistor
2022	Silicon, Springer	Design of Dopingless GaN Nanowire FET with Low 'Q' for High Switching and RF Applications
2022	Journal of Silicon, Springer.	Ashok Kumar Gupta and Ashish Raman, Performance Enhancement and Signal Distortion Analysis of Virtually Doped Nanotube Tunnel FET with Embedded Ferroelectric Gate Oxide
2022	International Journal of Numerical Modelling: Electronic Networks, Devices and Fields 35(2),e2960, Wiley	Effects of gate width variation on the performance of Normally-OFF dual-recessed gate MIS AlGaN/GaN HEMT
2022	Engineering Research Express, IOP Science	Investigation of variation in temperature on steep subthreshold slope nanowire tunnel field effect transistor based biosensor
2022	Transaction on Electrical and Electronics Material, Springer	Design and Investigation of Dual Dielectric Recessed-Gate AlGaN/GaN HEMT as Gas sensor Application
2022	IEEE Transactions on Electron Devices	CuO/Pentacene Type-II Planar Heterojunction for UV-Vis-NIR Photodetection with High EQE
2022	Transactions on Electrical and Electronic Materials	Design and Investigation of Dual Dielectric Recessed-Gate AlGaN/GaN HEMT as Gas sensor Application
2022	ECS Journal of Solid State Science and Technology, IOP Science	Charge-Plasma Based Cylindrical Nanowire FET for Low-Noise and High Sensing (in-press)
2022	Journal of Superlattices and Microstructures, Elsevier	Design and investigation of field plate-based vertical GAA –?-(AlGa)2O3/Ga2O3 high electron mobility transistor (in-press)
2022	Silicon, Springer	Ashok Kumar Gupta and Ashish Raman, Design Considerations and Optimization of Electrostatic Doped Ferroelectric Nanotube Tunnel FET: Analog and Noise Analysis
2021	Transaction on Electrical and Electronics Material	Dhruv Garg, Ashish Raman, Balwinder Raj and Grish Wadhwa, Surface Potential and Drain Current 2D Analytcal Modeling of Low Power Double Gate Tunnel FET
2021	Journal of Silicon, Springer	Rajneesh Sharma, Ashwani K. Rana, Shelza Kaushal, Justin B. King, and Ashish Raman, Analysis of Underlap Strained Silicon on Insulator MOSFET for Accurate and Compact Modeling
2021	Journal of Silicon, Springer	lubhawana okte, Ashish Raman, Balwinder Raj and Naveen Kumar, Junctionless Silicon Nanotube Tunnel Field-effect Transistor-based Resistive Temperature Detector
2021	Transactions on Electrical and Electronic Materials	Ranjan, R., Kashyap, N., Raman, A., Novel Vertical GAA-AlGaN/GaN Dopingless MIS-HEMT: Proposal and Investigation
2021	Journal of Electronic Materials, Springer	Gupta, A.K., Raman, A., Design, Investigation, and Sensitivity Analysis of a Biosensor Based on an Optimized Electrostatically Doped Nanotube TFET
2021	Journal of Silicon, Springer.	Shamshad Alam, Ashish Raman, Balwinder Raj, Sarabdeep Singh and Naveen Kumar,Design and analysis of Gate overlapped/underlapped NWFET based label free biosensor
2021	Journal of Silicon, Springer	Ashok Kumar Gupta and Ashish Raman, "Performance Enhancement and Signal Distortion Analysis of Virtually Doped Nanotube Tunnel FET with Embedded Ferroelectric Gate Oxide
2021	Journal of Silicon	Tweaking the Performance of Dopingless Nano-TFET with Misaligned Sandwiched Dual-Gate Structure

2021	Journal of Silicon	lubhawana okte, Ashish Raman, Balwinder Raj and Naveen Kumar, Junctionless Silicon Nanotube Tunnel Field Effect Transistor Based Resistive Temperature Detector
2021	Journal of Electronic Materials, Volume 50, Issue 9, Pages 5462 - 5471, Springer	Design, Investigation, and Sensitivity Analysis of a Biosensor Based on an Optimized Electrostatically Doped Nanotube TFET
2021	International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, Wiley	Effects of gate width variation on the performance of Normally-OFF dual-recessed gate MIS AlGaN/GaN HEMT (in-press)
2021	Journal of Silicon	Utkarsh Uppadhya, Ashish Raman and Ravi Ranjan and Naveen Kumar, Overlapped Gate-Source/Drain H-shaped TFET: Proposal, Design and Linearity Analysis
2021	Journal of Silicon	Design Considerations and Optimization of Electrostatic Doped Ferroelectric Nanotube Tunnel FET: Analog and Noise Analysis (in-press)
2020	Journal of Silicon, Springer.	Sarabdeep Singh and Ashish Raman, Design and Investigation of Pressure Sensor based on Charge Plasma Silicon NWFET with Cylindrical Gate Diaphragm
2020	Journal of Applied Physics A Springer, Vol - 126, 169: 1-9	Ravi Kumar, Nitesh Kashyap and Ashish Raman, High-Performance Dual Gate-Charge Plasma-AlGaN/GaN MIS-HEMT
2020	Superlattice and Microstructure Journal,Vol-111, pp- 518-528, Elsevier	Sarabjeet Kaur, Ashish Raman and R K Sarin, An Explicit Surface Potential, Capacitance and Drain Current Model for Double-Gate TFET
2020	Applied Physics A, Spinger, Vol-126, 441.	Deep Shekhar and Ashish Raman, Design and analysis of Dual-gate misalignment on the performance of Dopingless Tunnel Field Effect Transistor
2020	IEEE Transaction of Nanotechnology, Vol- 19, pp- 421 – 428	Naveen Kumar and Ashish Raman, Novel Design Approach of Extended Gate-on-Source based Charge-Plasma Vertical Nanowire TFET: Proposal and Extensive Analysis
2020	Journal of applied Physics A, Vol-126, 573 Springer	Ashok Kumar Gupta and Ashish Raman, Performance Analysis of electrostatic plasma-based dopingless Nanotube TFET
2020	IEEE Transaction of Nanotechnology	Naveen Kumar and Ashish Raman, Proscriptive Sensing Applications of Novel Hetromaterial based Dopingless Nanowire-TFET at Low Operating Voltage
2020	Journal of Silicon, Springer.	Ashok Kumar Gupta and Ashish Raman, Electrostatic-Doped Nanotube TFET: Proposal, Design, and Investigation with Linearity Analysis
2020	Journal of applied Physics A, Springer	Sarabjeet Kaur, Ashish Raman and R K Sarin, Analytical Modeling of Surface Potential, Capacitance and Drain Current of Heterojunction TFET
2020	Journal of Silicon, Springer.	Naveen Kumar and Ashish Raman, Novel Asymmetric Recessed-Gate/Source Architecture Advancement of Dual-Metal-Gate SiGe/Si Dopingless Nanowire-TFET for Low-Voltage Performance Optimization
2020	Journal of Silicon, Springer	Ashok Kumar Gupta, Ashish Raman and Naveen Kumar, Performance Tuning and Reliability Analysis of the Electrostatically Configured Nanotube Tunnel FET with Impact of Interface Trap Charges
2020	Transactions on Electrical and Electronic Materials, Springer	Ravi Ranjan, Nitesh Kashyap and Ashish Raman, “Novel Vertical GAA-AlGaN/GaN Dopingless MIS-HEMT: Proposal and Investigation
2020	Journal of Applied Physics A, Springer	Krishan Kumar, Ashish Raman, Balwinder Raj, Naveen Kumar and Sarabdeep Sing, Design and Optimization of Junctionless based Devices with Noise Reduction for Ultra-High Frequency Applications

2020	Superlattice and Microstructure Journal, Vol-111, pp- 518-528, Elsevier	Sarabjeet Kaur, Ashish Raman and R K Sarin, A Charge-based Capacitance Model for Double-Gate Hetero-Gate-Dielectric Tunnel FET
2020	IEEE VLSI Circuit and System Letter (TCVLSI)	Sarabdeep Singh, Ashish Raman and Sanjeev Kumar Sharma, Analysis of conventional doped and charge plasma dopingless Silicon Nanowire FET
2020	IEEE VLSI Circuits & Systems Letter (VCAL)	N.Shivaprasad, Ashish Raman, Deepak Bharti and Balwinder Raj, UV Photo Response of Semiconductor: Polymer blend Organic Field Effect Transistors
2019	IEEE Transactions on Electron Devices, ", Vol 66, Issue 10, pp-4453-4460, . (Impact Factor = 2.605)	Naveen Kumar and Ashish Raman, "Performance assessment of Charge-Plasma based Cylindrical GAA Vertical Nanowire-TFET with Impact of Interface Trap Charges
2019	Silicon Journal, Vol- 12, pp- 1-11, 1769–1777 Springer.	Prabhat Singh, Ashish Raman and Naveen Kumar, "Spectroscopic and Simulation Analysis of Facile PEDOT: PSS layer deposition-Silicon for Perovskite Solar Cell
2019	Journal of applied Physics A, Vol-125, 787, pp-1-11, Springer,	Ashish Raman, Manish Bansal, Naveen Kumar and Deepti Kakkar, "Design and Performance Analysis of GAA Schottky Barrier-Gate Stack-Dopingless Nanowire-FET for Phosphine Gas Detection
2019	Journal of Microsystem Technologies, Vol- 26, pp-1343–1350, Springer	Naveen and Ashish Raman, Low Voltage Charge-Plasma based Dopingless Tunnel Field Effect Transistor: Analysis and Optimization
2019	Journal of Silicon, Springer.	Ashok Kumar Gupta, Ashish Raman and Naveen Kumar, Cylindrical Nanowire-TFET with Core-Shell Channel Architecture: Design and Investigation
2019	Silicon Journal, Springer.	Naveen and Ashish Raman, Design and Analog Performance Analysis of Charge-Plasma based Cylindrical GAA Silicon Nanowire Tunnel Field Effect Transistor
2019	Journal of Super Lattice and Microstructure, Vol 125,pp-256-270, Elsevier, ISSN : 0749-6036 (2019)	Design and Analysis of Electrostatic-Charge Plasma based Dopingless IGZO Vertical Nanowire FET for Ammonia Gas Sensing", Journal of Super Lattice and Microstructure
2019	Journal of Nanoelectronics and Optoelectronics, Vol. 14, No-06, pp. 825–832 (2019).	Design and Analysis of Source Engineered with High Electron Mobility Material Triple Gate Junctionless Field Effect Transistor
2019	IEEE Transactions on Electron Devices, VOL 63, Issue 03, pp 1468-1474	Design and Investigation of Charge-Plasma based Workfunction Engineered Dual Metal-Heterogeneous Gate Si-Si0.55Ge0.45 GAA-Cylindrical NWTFET for Ambipolar Analysis
2019	Journal of applied Physics A, (Springer) (In-Press)	Nano Cantilever Tri-Gate Junctionless Cuboidal Nanowire-FET based Directional Pressure Sensor
2019	IEEE Transactions on Electron Devices (In-Press)	Design and Investigation of a Novel Charge Plasma based Core-Shell Ring-TFET: Analog and Linearity Analysis
2018	Journal of Nanoelectronics and Optoelectronics (ASP)	Design and Analysis of pressure sensor based on MEMS cantilever structure and pocket doped GD-TFET (In-Press)
2018	Journal of Computational Electronics, Springer, Vol-17, No. 3, pp- 967-976, 2018.	A Dopingless Gate All Around (GAA) Gate Stacked Nanowire-FET with reduced effect of parametric fluctuations
2018	IEEE Transactions on Electron Devices, vol. 65, no. 7, pp. 3026-3032, 2018.	Gate all around (GAA) charge plasma based dual material gate stack nanowire FET for enhanced Analog Performance
2017	Journal of Super Lattice and Microstructure, (elsevier)	A novel high mobility In1-xGaxAs cylindrical-gate-nanowire FET for gas sensing application with enhanced sensitivity

2016	Journal of Mobile Computing, Communications & Mobile Networks	Analysis and Comparison of Optimization Techniques for Interference Duration in Cognitive Radio
2016	Int. J. Information and Communication Technology	Design and analysis of RF-low power and low-phase noise CMOS ring oscillator for fully integrated RF communication systems technologies
2016	Journal of Superlattices and Microstructures", (elsevier)	Pressure sensor based on MEMS nano-cantilever beam structure as a heterodielectric gate electrode of dopingless TFET
2016	Journal of Semiconductor, (IOP-Science)	Dual Material Gate Based DG-IMOS: Design and Optimization Analysis
2015	Wulfenia Journal	A 180 nm Transmission Gate Based Micro-Power Ring Oscillator for Wireless Telemetry Applications
2015	Journal of VLSI Design Tools and Technology	A Review on Charge Pump Circuits for PLL Applications
2015	Journal of Electronics Design and Technology	Designing of Low Power Charge Pump Circuit with Minimum Current Mismatch for High Speed PLL Applications
2015	Recent Trends in Sensor Research & Technology Journal	Optimization of Sensing Parameters Using PSO, GA Algorithms for Cognitive Radio
2013	International Journal of Advanced Science and Technology (IJAST), (SERSC)	Design and Investigative Aspects of RF-Low Power 0.18 ?m based CMOS Differential Ring Oscillator
2013	International Journal of Engineering Research & Technology	Phase and Frequency Detector For Low Jitter And High Speed Applications-Review
2013	Int. J. Biomedical Engineering and Technology (Inderscience)	The design of a novel delay cell based 8.3 GHz, low phase noise ring oscillator in C-MOS 180 nm technology for biomedical ultra-wide-band integrated applications

Conference Publications :

Year	Conference	Publication
2021	12th International Conference on Advances in Computing, Control, and Telecommunication Technologies, ACT 2021	A comparative study on different proposed nanotube TFETs
2020	7th International Conference on Signal Processing and Integrated Networks, SPIN 2020	Design and implementation of high-speed universal asynchronous receiver and transmitter (UART)
2020	11th International Conference on Advances in Computing, Control, and Telecommunication Technologies, ACT 2020	Study of improved topologies of nanowire MOSFET: Solution to doping control issues
2020	11th International Conference on Advances in Computing, Control, and Telecommunication Technologies, ACT 2020	A review on organic fieldeffect transistors
2020	7th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering, UPCON 2020	Current Starved Ring Voltage Control Oscillator for High Frequency and Low Power Application
2019	IEEE, International Conference on Signal Processing and Integrated Networks, SPIN 2019	Linearity Analysis of Gate Engineered Dopingless and Junctionless Silicon Nanowire FET
2019	6th International Conference on Signal Processing and Integrated Networks, SPIN 2019	Low Power and High Frequency Voltage Controlled Oscillator for PLL Application
2019	6th International Conference on Signal Processing and Integrated Networks, SPIN 2019	Design and Analysis of Novel Charge-Plasma Based Dopingless U-Shaped FET
2019	IEEE Conference Recent trends in electroncs and Computer Science	Analysis of Linearity Parameters for gate all around (GAA) Charge Plasma and Junctionless NWFET

2019	IEEE Conference Recent trends in electroncs and Computer Science	Linearity Analysis of Charge-Plasma based Dopingless Si0.55Ge0.45-Silicon Dual Gate-Tunnel Field Effect Transistor
2018	2nd IEEE International Conference on Trends in Electronics and Informatics, ICOEI 2018	Multiband Microstrip Patch Antenna Design for 5G Using Metamaterial Structure
2015	International Conference on Electrical, Electronics, Signals, Communication and Optimization	Designing of Phase and Frequency Detector for low Jitter and high speed applications
2012	International Conference of Electrical and Electronics Engineering, World Congress Engineering (WCE-2012) London	A RF Low Power 0.18-um based CMOS Differential Ring Oscillator
2012	Intl. Conf. on Advances in Electronics, Electrical and Computer Science Engineering	A DA Serial Multiplier Technique based on 32- Tap FIR Filter for Audio Application
2010	International conference on Information and Multimedia Technology, Hongkong	Design and Implementation of Low Power Chip Uniprocessor using GALS Design Style
2010	International Conference on Biomedical Engineering and Assistive Technologies	A Time-Power Efficient Decimator using Vedic Algorithm
2010	International Conference on Biomedical Engineering and Assistive Technologies	High Speed and Low Offset Comparator for A/D Converter

Book/Chapter Publications :

Type	**Title**	**Publisher**	**Authors**	**ISBN/ISSN No.**	**Year**
Book Chapter	HumanMachine Interface-Based Robotic Wheel Chair Control	Futuristic Design and Intelligent Computational Techniques in Neuroscience and Neuroengineering	Deepti Kakkar and Ashish Raman	9781799874348	2022
Book	Sub-micron Semiconductor Devices: Design and Applications	CRC Press (T&F)	Ashish Raman, Deep Shekhar, Naveen Kumar	9780367648091	2022
Book Chapter	Multi-Quantum Well-Based Solar Cell	Electrical and Electronic Devices, Circuits, and Materials: Technological Challenges and Solutions, Wiley	Ashish Raman, Chetan Chaturvedi, Naveen Kumar	9781119755104	2021
Book Chapter	High-Frequency CNTFET-Based VoltageControlled Oscillator for PLL Application	Lecture Notes in Networks and Systems, Volume 106, Pages 413 - 419	Yogesh Kumar, Ashish Raman, Ravi Ranjan, and R K Sarin	2367-3389	2020
Book Chapter	A Low-Power Hybrid VSCNTFET-CMOS Ring VoltageControlled Oscillator Using Current Starved Power Switching Technology	Nanoscale VLSI, Springer	Ashish Raman, Vikas Kumar, Malav, Ravi Ranjan, R. K. Sarin	978-981-15-7937-0	2020

Book Chapter	Distance based Enhanced Threshold Sensitive Stable Election routing Protocol for Heterogeneous Wireless Sensor Network	Springer. (In Press)	Richa Rani, Deepti Kakkar, Parveen Kakkar, Ashish Raman	978-3-662-57277-1	2019
Book Chapter	Design and analysis of memristor based DRAM cell for low power application	VLSI AND Post CMOS Electronics, Volume 1: Design, Modeling and Simulation (IET)	Ashish Raman, Deepshekhar, Ravi Ranjan and Suchitra Kumari	978-1-83953-051-7	2019

Research Projects :

Role	Project Type	Title	Funding Agency	From	To	Amount	Status	Co-Investigator
Co-Chief Investigator	R&D Major	SMDP-C2SD	MeitY	2015	2021	99.1 Lakhs	Completed	Dr Mamta Khosla
	Research Infrastructure Development	FIST-Charaterisation of Semiconductor Devices	DST-FIST	2015		165 Lakhs	Ongoing	
CO-PI at NITJ	Research under Exchange Program	Aalto-IITI cooperation for the skill developments of IoT based implementation	CIMO Asia programme jointly with Aalto University, Finland and IIT Indore, India	2016	2018	40000 Euro's	Completed	
Principle Invistegtor	R&D Major	FPGA based High Speed CCSDS Processor for Baseband Receiver	ISRO	2020	2022	15.90 lakhs	Ongoing	
Supervisor	R&D Minor	Design and analysis of Characterization of Ga2O3 si tendam junction for high power application,	TEQIP-III	2018	2019	0.40 Lakhs	Completed	
Supervisor	R&D Minor	Design and analysis of efficient pervoskite Solar cell	TEQIP-III	2017	2018	0.60 Lakhs	Completed	

Principle Investigator	R&D Major	Modeling and analysis of quantum Effect for Sub- 10 node Nanowire based devices	SERB, DST, New Delhi.	2021	2024	Lakhs	Ongoing	
PI	Research	Visvesvaraya PhD fellowship for Electronics and IT Phase-I	Media Lab Asia under Ministry of Communication and IT (MCIT)	2016	2021	50.06 Lakhs	Completed	
Noda Offcer/PI	Research	Visvesvaraya PhD fellowship for Electronics and IT Phase -II	Ministry of Electronics and IT (MeitY)			1.3 Cr	Ongoing	
PI/Coodinator	Research and manpower	inup-i2i as Collaborative patner of IIT Delhi	MeitY	2023			Ongoing	

Events Organized :

Category	Type	Title	Venue	From	To	Designation
Self Financed Short Term Course	National	Electronics and Communication Systems Design Aspects	ECE, NIT Jalandhar	25-05-2015	29-05-2015	Coordinator
Training program	International	10 days training program on “Research-Teaching Exchange Excursion Workshop” jointly organized by Dept. of ECE, NIT Jalandhar and Techical University of Munich, Germany,	VLSI Design Lab, ECE Dept. NIT Jalandhar	15-09-2016	24-09-2016	Coordinator
STC, TEQIP-II	National	Recent Trends in VLSI AND Communicaiton Systems	ECE, NIT Jalandhar	17-06-2013	21-06-2013	Coordinator
Expert Talk	National	Process Integration Issues in Advance CMOS node	VLSI Lab, NITJ	08-04-2016	08-04-2016	Coordinator
Expert Talk	National	Nano Scale Devices	VLSI Lab, NITJ	29-03-2016	29-03-2016	Coordinator
Expert Talk	National	VLSI State of Art	VLSI Lab, NITJ	12/09/2013		Coordinator
STC	National	Recent Trends in Biomedical Signal Processing and VLSI Design		30/05/2019	03/06/2019	Coordinator

Conference	National	Innovation in Applied Science and Engineering (NCIASE-2019)	NIT Jalandhar	27/04/2019	28/04/2019	Organizing Secretary
One-week Self Financed Short Term Course	National	“Research Trends in VLSI Devices and Circuits Co-design” held from 4th to 8th May-2018	VLSI Design Lab, NIT Jalandhar	04-05-2018	08-05-2018	Coordinator
STC	National	NanoScience for Engineering Applications	STC on Recent Trends in Jointly organized with NITTTR Chandigarh (Sponsored by TEQIP-III)	22/06/2020	26/06/2020	Coordinator
STC	National	Recent Trends in Advances in Communication Systems for Integrated Technology during (Sponsored by TEQIP-III)	NIT Jalandhar	06/07/2020	10/07/2020	Coordinator
STC	National	Recent Trends in Artificial Intelligence and its Applications	Jointly organized NIT Jalandhar and NITTTR Chandigarh (Sponsored by TEQIP-III)	27/07/2020	31/07/2020	Coordinator
STC	National	Sub-micrometer Semiconductor Device to Circuit Co-Design and Modelling Techniques	NIT Jalandhar	20/08/2020	24/08/2020	Coordinator
STC	National	IOT and Its Applications	Jointly organized NIT Jalandhar and NITTTR Chandigarh (Sponsored by TEQIP-III)	07/09/2020	11/09/2020	Coordinator
STC	National	Resent Trends in Advanced Materials and Devices	NIT Jalandhar	21/09/2020	25/09/2020	Coordinator
STC	National	Communication Strategies and Statistical Applications	NIT Jalandhar (Sponsored by TEQIP-III).	23/09/2020	27/09/2020	Coordinator
Conference	National	National Conference of Innovation in Applied science and engineering	NIT Jalandhar	27/04/2019	28/04/2019	Coordinator/ Organizing Secretary

Conference	National	International Conference on Computing Communication Signal Processing	NIT Jalandhar	23/07/2020	24/07/2020	Coordinator/ Organizing Secretary
Symposium	International	International Symposium on Semiconductor Materials and Devices	NIT Jalandhar (Jointly organized with semiconductor society of India)	31/10/2020	02/11/2020	
STC	National	STC on Role of Leadership in Higher Education	Jointly organized NIT Jalandhar and NITTTR Chandigarh.	14/12/2020	18/12/2020	Coordinator

Professional Affiliations :

Designation	Organization
Member	IEI
Member	IEEE Electron Devices Society Membership
Member	IEEE Solid-State Circuits Society Membership
Member	IACSIT
Member	IAENG

PhD Supervised :

Scholar Name	Research Topic	Status	Year	Co-Supervisor
Mr Ashok Kumar Gupta	DESIGN AND PERFORMANCE OPTIMIZATION OF ELECTROSTATIC DOPED NANOTUBE TFET AND ITS SENSOR APPLICATION	Submitted	2022	
Ms. Sarabjeet Kaur	Analytical Modeling and Performance Improvement of Tunnel Field Effect Transistor	Awarded	2022	Dr R K Sarin
Mr Soumya Sen	Design and Performance Analysis of Electrostatic Doped Heterostructure Nanotube TFET and its Applications	Ongoing	2021	Dr Mamta Khosla
Mr. Sarabdeep Singh	Design and Analysis of Charge Plasma based Nanowire FET and its Sensor Application	Awarded	2021	
Mr. Naveen Kumar	Design and Performance Optimization of Dopingless GAA-Nanowire TFET and its Sensor Application	Awarded	2021	
Mr. Sahil Sankhyan	Nanoelectronics	Ongoing	2021	Dr Mamta Khosla
Mr Abhishek Singh Chauhan	NanoSheet FET	Ongoing	2021	
Mr Ankit Kumar Maurya	Design and Fabrication of Miniaturized Circularly Polarized Planar Antenna for Wireless Applications	Ongoing	2020	Dr Nitesh Kashyap
Mr Ravi Ranjan	Design and Investigation of Normally-OFF HEMT for enhanced performance parameter	Ongoing	2018	Dr Nitesh Kashyap
Mr Deep Shakhar	DESIGN, ANALYSIS AND OPTIMIZATION OF MISALIGNED DUAL GATE DOPINGLESS TUNNEL FIELD EFFECT TRANSISTOR FOR ITS CIRCUIT APPLICATION	Ongoing	2018	

PG Dissertation Guided :

Student Name	Dissertation Title	Status	Year	Co-Supervisor
Utkarsh Upadhaya	Overlapped Gate-Source/Drain H-shaped Nanotube TFET: Proposal, Design and Linearity Analysis	Completed	2021	
Kilaru Sumanth Krishna	Performance analysis of normally-off AlGaN/GaN HEMT	Completed	2021	Dr Deepti Kakkar
Saumya Tripathi	Pentacene /Cuo Type-II Hetrojunction for UV-Vis-NIR Photodetection	Completed	2021	
Madhu Varsha BhupathiRaju	Implementation and Optimization of Syndrome Calculator for Reed Solomon Decoder	Completed	2021	Dr Deepti Kakkar
Krisum Raj Purkait	P-Doped ?-Ga2O3 on Aln/ ?-Ga2O3 normally of HEMT	Completed	2021	Dr Indu Saini
Kanika Gupta	Design of Low Power Bit Swapping BIST for IC Self Testing	Completed	2021	
K. Jaswanth Kumar	Investigating the performance of Vertical nanowire TFET with source delta doping	Completed	2021	
Apoorva Srivastava	Design and Analysis of Ultra High Aspect Ratio InGaAs FinFET	Completed	2021	Dr Indu Saini
Dhruv Garg	Surface Potential and Drain Current 2D Analytical Modeling of Low Power Double Gate Tunnel FET	Completed	2020	Dr Balwinder Raj
Krishan Kumar	Design and Analysis of Junctionless FETs Based Devices for Noise Optimization	Completed	2020	Dr Balwinder Raj
Lubhawana Okte	Junctionless Silicon Nanotube Tunnel Field Effect Transistor based Resistive Temperature Detector	Completed	2020	Dr Balwinder Raj
Nibha Kumari	Design and Analysis of eterodielectric Dual Material Gate Dopingless Nanowire FET	Completed	2020	Dr Deepti Kakkar
Shashank Tiwari	FPGA Based High Speed CCSDS Processor: Frame-Synchronizer and De-Randomiser for BaseBand Receiver	Completed	2020	
N. Shivaprasad	UV Photo Response of Organic Transistors with TIPS-Pentacene: PS Blend and HfO2-PVP Bilayer Dielectric	Completed	2020	
Shamshad Alam	Design and Analysis of Gate Ovrlapped/Underlapped NWFET Based-Label Free Biosensor for Glicose Detection	Completed	2019	Dr Balwinder Raj
Yogesh Kumar	Design and Analysis of Differential Voltage Controller Oscillator Based on Dual Delay Technique for PLL Application	Completed	2019	Dr R K Sarin
Ashok Kumar Gupta	Negative Capacitance Charge Plasma based Ring-FET: A Novel Structure with Scaled Operating Voltage	Completed	2019	
Jarupula Venkat Sai Prasad	Label Free Biosensor Based on Organic Nanowire Field Effect Transistor	Completed	2019	
Soumya Prasanna Chattopadhyay	Design and Investigation of Gallium Nitride based High Electron Mobility Transistor with Recessed Gate Structure employing Dual Gate Insulator for Carbon Monoxide (CO) Sensing Application	Completed	2019	

Neha Jayaswal	Design and Analysis of Electrostatic Charge Plasma based Dopingless IGZO Vertical Nanowire FET for Ammonia Gas Sensing	Completed	2018	
Vikas Kumar Malav	A Low Power Hybrid VS-CNTFET-CMOS RVCO using Current Straved Power Switching Technology	Completed	2018	Dr R K Sarin
Prabhat Singh	Design and Analysis of Efficient Prevoskite Solar Cell	Completed	2018	
Manish Bansal	Perfrormance Analysis of Different Catautic Metals in Gate All Around Schottky Barrier NanoWire MOSFET for Phosphine GAS Detection	Completed	2018	Dr Deepti Kakkar
Aman Aggarwal	Pressure Sensor based on MEMS Nano Cantilever embedded on Triple Gate Junctionless Nanowire FET (TG- JL NWFET)	Completed	2018	
Shivangi Shringi	Design And Analysis Of Triple Gate Junction Less Fet With High Electron Mobility Material	Completed	2017	
Navaneet Kumar Singh	Design And Analysis Of High Mobility In1-Xgaxas Gate-All-Around For Gas Sensing Application With Enhanced Sensitivity	Completed	2017	
Chetan Chaturvedi	Comparative Analysis And Impact Of Heterojunction Materials In 25 Layers Multi-Quantum Well Based Solar Cells.	Completed	2017	
Rathod Vikendra	Human Machine Interface Based Robotic Wheel Chair Control Using P300 Wave And Support Vector Machine	Completed	2016	Dr Deepti Kakkar
Amit Kumar Vijay	Comparative Analysis Of Optimization Technique For Interference Duration In Cognitive Radio	Completed	2016	
Suchitra Kumari	Design And Analysis Of Dram Memory Cell Using Memeristor And Transmission Gate	Completed	2016	
Gagan Kumar	Design And Analysis Of Pressure Sensor Based On MEMS Cantilever Structure And Doping-Less TFET	Completed	2016	
Tanya Singh Chauhan	De-Noised Wavelet Packet Entropy Based Spectrum Sensing In Cognitive Radios	Completed	2016	
Deep Shekhar	Designing Of Low Power Charge Pump Circuit With Minimum Current Mismatch For High Speed PLL Applications	Completed	2015	
Jitendra Krishna Arya	Design Of Novel CMOS 5t-Sram Cell For Low Power Consumption And Small Area Application In 65nm Technology	Completed	2015	
Juttu Ramesh	Optimization Of Sensing Parameters Using Pso, Ga Algorithms For Cognitive Radio	Completed	2015	
Atul Goyal	Optimization Of BER For Sdr In Cognitive Applications Using BBO And PSO Techniques	Completed	2014	
Abhishek Singh	Throughput Optimization In Cooperative Communication Network With Or Fusion Rule Using BBO And PSO Algorithms	Completed	2014	Dr Deepti Kakkar
Prabhod Singh	Design Of 7t Sram Cell For Low Power High Stability And High Density Applications	Completed	2014	

Rajasekhar	Design And Analysis Of Pressure Sensor Based On MEMS Cantilever Structure and Pocket Doped DG-TFET.	Completed	2014	
Inderdeep Singh	Design Of Temperature Nanosensor By Using The Electronic-Transport Properties Of Graphene Nanoribbon	Completed	2013	
Siva Sankar Prasad D	Designing Of Phase And Frequency Detector For Video Application	Completed	2013	Dr R K Sarin
Lesh Kumar Patel	Design And Implementation Of High Performance CMOS Current Comparator For Adc Applications	Completed	2013	
Dinesh Chand Gupta	Design Of Low Power SRAM Cell Using Leakage Current Reduction Techniques In 90 nm CMOS Technology.	Completed	2012	
K Balraj	Design Of A High Performance Reconfigurable Fir Filter Using Baugh-Wooley Algorithm	Completed	2012	
Chandan Singh	Designing Of A High Speed High Resolution Preamplifier Latch Comparator Using Self-Biased Differential Amplifier	Completed	2011	
Vignesh.V	ASIC Implementation Of A Reconfigurable Decimation Filter Using Vedic Algorithm	Completed	2011	
Anvesh Kumar	Design And Implementation Of Reconfigurable FFT Through Vedic Mathematics	Completed	2010	Dr Arun Khosla
Prakash Chand Joshi	ASIC Implementation And Power Optimization For RISC Processor Using Gals Technique	Completed	2010	
Subvesh Raichand	High Throughput Fir Filter Using Distributed Arithmetic	Completed	2009	

Patents :

Name	Reg./Ref. No.	Date of Award/Filling	Organization	Status
A Normally-on Dual Gate (DG) AlGaN/GaN High Electron Mobility Transistor Device		2022		Granted

Admin. Responsiblities :

Position Held	Organization	From	To
Additional Warden Hostel No 6 (Boys)	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Institute Level)	31/07/2012	30/10/2012
Warden Hostel No 3 (Boys)	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Institute Level)	31/10/2012	08/07/2013
Warden Mega Hostel Boys	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Institute Level)	09/07/2013	01/09/2014
Warden Mega Hostel Boys and Mess	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Institute Level)	Jan 2015	07/03/2017
Warden Mega Hostel Boys Block B (Additional Charge)	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Institute Level)	09/03/2017	20/09/2017
Warden Hostel No 2 (Boys)	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Institute Level)	07/03/2017	Feb 2018
Assistant Proctor	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Institute Level)	Feb 2011	June 2012

Faculty Counselor	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Institute Level)	19/02/2015	
Counselor to B.Tech 1st year student	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Institute Level)	04/09/2017	
Time Table Coordinator	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Departmental Level)	Aug 2009	July 2012
M.tech VLSI Design Coordinator	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar	Aug 2011	
B.Tech 1st Year Coordinator	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Departmental Level)	Aug 2016	2017
Departmental Library Incharge	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Departmental Level)	Aug 2015	July 2017
Society OF Electronics and Communication Engineers	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Departmental Level)	Aug 2015	Till
Industrial Training In-charge	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Departmental Level)	Aug 2011	July 2012
Member of Departmental BOS	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Departmental Level)	2007	Till
Institute Time Table Co-Incharge	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar (At Institute Level)	Dec 2012	Till
Warden	NIT Jalandhar	Jan, 2019	July 2019
NSS, Group Coordinator	NIT Jalandhar	Oct 2018	till
Nodal Officer Vishvariya PhD Scheme	NIT Jalandhar	2020	Till
NBA- Institute Coordinator	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar	March 2021	Till Date
IQAC	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar	July 2021	Till Date
Associate Dean (R&C)	Dr. B.R. Ambedkar National Institute of Technology, Jalandhar	February 23	Till Date

Award and Honours :

Title	**Activity**	**Given by**	**Year**
Keynote Speaker	Research Mythology and its Use in Education at MIT Moradabad (FDP is sponsored by AKTU University, Lucknow.)	MIT Moradabad (FDP is sponsored by AKTU University, Lucknow.)	2020-21
Expert Talk	Advances in Electrical & Electronics Engineering	NITTTR Chandigarh	2020
Plenary Talk	International Conference on Computing Communication Signal Processing	NIT Jalandhar	2020
Session Chair	International Conference on Computing Communication Signal Processing	NIT Jalandhar	2020
Expert talk	Fundamentals and Advances in CMOS VLSI Design	G H Raisoni College of Engineering Nagpur	2020
Expert talk	Fundamentals and Advances in CMOS VLSI Design	at Indraprastha Engineering College Ghaziabad	2020

Expert Talk	Low Power VLSI Design for Communication Systems and Networks (LVCSN'20)	NIT Jalandhar	2020
Expert Talk	FDP on Analog/Mixed VLSI circuits for Brain Machine Interface (FDP is sponsored by All India Council of Technical education (AICTE) under the scheme "AICTE Training and Learning" (ATAL))	National Institute of Technology, Silchar	2020
Resource Person	Expert talk on “Current Trends in PLL and Oscillator Design for Integrated Applications”, (STTP is sponsored by All India Council of Technical education (AICTE).	SGSITS, Indore	2020
Resource Person	Expert talk on “Current Trends in PLL and Oscillator Design for Integrated Applications”, (STTP is sponsored by All India Council of Technical education (AICTE).	SGSITS Indore	2020
Resource Speaker	International COnfrence recent trends on electrons and computer science at NIT Silchar	NIT Silchar	2019
Session Chair	International Conference recent trends on electrons and computer science at NIT Silchar	NIT Silchar	2019
Session Chair	National Conference of Innovation in Applied Science and Engineering	NIT Jalandhar	2019
Resource Speaker	National Conference of Innovation in Applied Science and Engineering	NIT Jalandhar	2019
Expert Lecture	STC on Recent Trends of Biomedical Signal Processing and VLSI Design	NIT Jalandhar	2019
Expert Lecture	Applications of Machine Learning in SiGnal Image & Computer Vision	Bipin-Trapathi Kumaon Institute of Technology, Dwarahat, Almora.	2019
Expert Lecture	Faculty Development Program on Integrated Circuits	MIT Moradabad	2018
Expert Lecture	Workshop on “Hands-on Session on VLSI Design” at NIT Delhi	NIT Delhi	2017
Expert Lecture	School of VLSI Design and Embedded System NIT Kurukshetra	NIT Kurukshetra	2017