Profile Page

Name	:	Dr Balwinder Raj
Designation	:	Associate Professor
Department	:	Electronics and Comm. Engg.
Qualification	:	Postdoc-2011 VLSI Design (University of Rome, Italy) Ph.D-2010 Microelectronics and VLSI Design (IIT Roorkee) M.Tech-2006 Microelectronics (Panjab University Chandigarh) B.Tech-2004 Electronics Engineering (Punjab Technical University)
Address	:	Department of ECE NIT Jalandhar Jalandhar, Punjab - 144011
Email	:	rajb@nitj.ac.in
Phone	:	+91-7589480655

Research Interests :

Microelectronics and VLSI Design: Novel Semiconductor Devices, Classical/Non-Classical Nanoscale Devices Modeling, Ultra Low Power VLSI/ULSI Design and Technology, Nanoscale Memory Design, Digital VLSI Circuit Design, and Reconfigurable FPGA Implementation

Other Profile Links :

Google Scholar Link :

Dr. Balwinder Raj Click Here

Journal Publications :

Year	Journal	Publication
2019	Indian Journal of Pure & Applied Physics (IJPAP), Vol 57, PP 352-360	Neeraj Jain, Balwinder Raj, “Thermal Stability Analysis and Performance Exploration of Asymmetrical Dual-k underlap Spacer (ADKUS) SOI FinFET for Security and Privacy Applications
2019	Applied Physics A, Springer, VOL. 125, NO.3, pp. 203.1 to 203.11	Jeetendra Singh, Balwinder Raj, “Tunnel Current Model of Asymmetric MIM Structure Levying Various Image Forces to Analyze the Characteristics of Filamentary Memristor”,
2019	IEEE Transactions on Very Large Scale Integration Systems (Accepted)	Jeetendra Singh, Balwinder Raj, “Design and Investigation of 7T2M NVSARM with Enhanced Stability and Temperature Impact on Store/Restore Energy

2019	Microelectronics Journal, Elesvier, Volume 85, Pages 17-24, March 2019	Amandeep Singh, Mamta Khosla, Balwinder Raj, “Design and Analysis of Dynamically Configurable Electrostatic Doped Carbon Nanotube Tunnel FET",” Microelectronics Journal, Elesvier, Volume 85, Pages 17-24, March 2019
2019	American Scientific Publishers, Vol. 14, PP. 349–359	Neeraj Jain and Balwinder Raj, “Dual-k Spacer Region Variation at the Drain Side of Asymmetric SOI FinFET Structure: Performance Analysis towards the Analog/RF Design Applications”, communicated in “Journal of Nanoelectronics and Optoelectronics”
2018	IEEE Nanotechnology, Vol. 17, No. 2, PP. 268-267	Jeetendra Singh, Balwinder Raj, "Modeling of Mean Barrier Height Levying Various Image Forces of Metal Insulator Metal Structure to Enhance the Performance of Conductive Filament Based Memristor Model”
2018	IEEE Sensor Journal, VOL. 18, NO. 15	Girish Wadhwa, Balwinder Raj, "Parametric Variation Analysis of Charge-Plasma-based Dielectric Modulated JLTFET for Biosensor Application"
2018	IEEE/IET Circuits, Devices & Systems, Vol. 12, PP. 638 – 64	Gurmohan Singh, R. K. Sarin and Balwinder Raj, “Fault-Tolerant Design and Analysis of Quantum-Dot Cellular Automata Based Circuits”,
2018	Journal: Engineering Science and Technology, an International Journal, Elsevier's, Vol. 21, PP-862-868	Jeetendra Singh, Balwinder Raj, "Temperature Dependent Analytical Modeling and Simulations of Nanoscale Memristor
2018	Journal of Electronic Materials (JEMS), Springer, Volume 47, Issue 8, pp 4683–4693	Girish Wadhwa, Balwinder Raj, "Label Free Detection of Biomolecules using Charge-Plasma-Based Gate Underlap Dielectric Modulated Junctionless TFET"
2018	JoS, IoP, Vol. 39, No. 7, PP. 074006-1-12	Jeetendra Singh, Balwinder Raj, "Comparative Analysis of Memristor Models for Memories Design”
2018	JNO, ASP, Vol. 13, PP 1473-1477	Jeetendra Singh, Sanjeev Sharma, Balwinder Raj, Mamta Khosla Analysis of barrier layer thickness on performance of In1-xGaxAs based Gate Stack Cylindrical Gate Nanowire MOSFET, ”
2018	Sensor Letter, ASP, Vol. 16, PP. 374–385	Divya Yadav, Shailesh Singh Chouhan, Santosh Kumar Vishvakarma and Balwinder Raj, " Application Specific Microcontroller Design for IoT based WSN”
2018	Opto-electronics Journal, Elsevier, Volume 26, Issue 2, Pages 141-148	Aakash Jain, Sanjeev Sharma, Balwinder Raj, “Analysis of Triple Metal Surrounding Gate (TM-SG) III-V Nanowire MOSFET for Photosensing Application”,
2018	Journal of Computational Electronics, Springer, Volume 17, Issue 1, pp 138–145	G. Saiphani Kumar, Amandeep Singh, Balwinder Raj, “Design and Analysis of Gate All Around CNTFET based SRAM cell Design”,
2017	Journal of Nanoelectronics and Optoelectronics, American Scientific Publishers, USA, Vol.12, PP. 171–176, 2017.	“Subthreshold Performance of In1-xGaxAs based Dual Metal with Gate Stack Cylindrical/Surrounding Gate Nanowire MOSFET for Low Power Analog,
2017	IEEE VLSI Circuits and Systems Letter, Volume3, Issue2, June 2017	“Estimation of Stability and Performance metric for Inward Access Transistor based 6T SRAM Cell Design using n-type/p-type DMDG-GDOV TFET”
2017	Journal of Materials Science: Materials in Electronics, Springer, Vol.28, PP. 1762–1768, 2017	“Analysis of Electrostatic Doped Schottky Barrier Carbon Nanotube FET for Low Power Applications,”
2017	International Journal of Electronics and Communications, (AEÜ), Elsevier, Vol. 80, PP.67–72, 2017.	Amandeep Singh, Mamta Khosla, Balwinder Raj, “Design and Analysis of Electrostatic Doped Schottky Barrier CNTFET Based Low Power SRAM,”

2017	Indian Journal of Pure & Applied Physics (IJPAP), Vol. 55, pp. 97-103, February 2017	Gurmohan Singh, R. K. Sarin and Balwinder Raj, “Design and Performance Analysis of a New Efficient Coplanar Quantum-Dot Cellular Automata Adder”,
2017	Journal of Microprocessors and Microsystems, Elsevier, Vol. 52, PP.59-68, May 2017	Gurmohan Singh, R. K. Sarin and Balwinder Raj, “Design and Analysis of Area Efficient QCA Based Reversible Logic Gates”,
2017	Journal of Computational Electronics, Springer, Volume 16, 2017	“Design and Analysis of Gate All Around CNTFET based SRAM cell Design”,
2016	Journal of Nanoelectronics and Optoelectronics, American Scientific Publishers, USA, Vol.11, PP. 323-333, June 2016.	“Analysis of ION and Ambipolar Current for Dual-Material Gate-drain Overlapped DG-TFET,”
2016	Journal of Semiconductors (JoS), IOP Science, Vol.37, PP. 104001-8, Oct 2016	“Compact Model for Ballistic Single Wall CNTFET under Quantum Capacitance Limit,”
2016	Journal of Computational Electronics, Springer, Volume 15, Issue 2, PP. 455-465, June 2016	A Novel Robust Exclusive-OR Function Implementation in QCA Nanotechnology with Energy Dissipation Analysis
2016	Journal of Electronic Materials, Springer, Vol. 45, Issue 12, pp 4825-4835, 2016	Circuit Compatible Model for Electrostatic Doped Schottky Barrier CNTFET
2016	Journal of Semiconductors (JoS), IOP Science, Vol.37, PP. 074001-6, July 2016	Modeling and Simulation of Carbon Nanotube Field Effect Transistor and its Circuit Application
2016	Microelectronics Journal, Elsevier, Vol. 53, PP. 65-72, 2016	A Gaussian Approach for Analytical Subthreshold Current Model of Cylindrical Nanowire FET with Quantum Mechanical Effects
2016	Journal of Nanoelectronics and Optoelectronics, American Scientific Publishers, USA, Vol. 11, PP. 388-393, 2016	Comparative Analysis of Carbon Nanotube Field Effect Transistor and Nanowire Transistor for Low Power Circuit Design
2015	Journal of Computational Electronics, Springer Vol. 14, No. 2, pp.820-827, July 2015	Compact channel potential analytical Modeling of DG-TFET based on Evanescent–mode Approach
2015	Journal of Electronic Materials, Springer, Vol. 44, Issue 12, pp 4825-4835, Dec 2015	Temperature Dependent Modeling and Performance Evaluation of Multi-Walled CNT and Single-Walled CNT as Global Interconnects
2015	Journal of Computational Electronics, Springer, Volume 14 Issue 2, pp. 469-476, June 2015	Performance and analysis of temperature dependent Multi-walled Carbon Nanotubes as Global Interconnects at different technology nodes
2015	Journal of Materials Science: Materials in Electronics. Springer, Vol. 26, No. 8, pp. 6134-6142, 2015	Influence of Temperature on MWCNT bundle, SWCNT bundle and Copper interconnects for Nanoscaled Technology nodes
2014	Microelectronics Reliability, Elsevier, Vol. 54, pp 90-99, 2014	PVT variations aware low leakage INDEP approach for nanoscale CMOS Circuits
2014	, Taylor & Francis, Vol. 101, issue 1, pages 61-73, 2014	ONOFIC Approach: Low Power High Speed Nanoscale VLSI Circuits Design
2014	International Journal of Electronics, Taylor & Francis, Vol.102, No.2, pages 200-215, 2014	INDEP approach for leakage reduction in nanoscale CMOS circuits

2013	Journal of Material Science in Semiconductor Processing, Elsevier, Vol. 16, issue 4, pp. 1131- 1137, 2013.	Quantum Mechanical Analytical Modeling of Nanoscale DG FinFET: Evaluation of Potential, Threshold Voltage and Source/Drain Resistance
2011	IEEE Circuits and System Magazine, vol. 11, issue 2, pp. 38-50, 2011	Nanoscale FinFET Based SRAM Cell Design: Analysis of Performance metric, Process variation, Underlapped FinFET and Temperature effect
2011	Journal of Low Power Electronics (JOLPE), Academy Publisher, FINLAND, vol. 7, issue 2, pp. 163-171, 2011	Process Variation Tolerant FinFET Based Robust Low Power SRAM Cell Design at 32nm Technology
2009	Microelectronics International, UK, vol. 26, pp. 53-63, 2009.	Analytical Modeling for the Estimation of Leakage Current and Subthreshold Swing Factor of Nanoscale Double Gate FinFET Device"
2008	Journal of Nanoelectronics and Optoelectronics (JNO), USA, vol. 3, no. 2, pp. 163-170, 2008.	A Compact Drain Current and Threshold Voltage Quantum Mechanical Analytical Modeling for FinFETs"

Conference Publications :

Year	Conference	Publication
2019	NCIASE-2019, NIT Jalandhar, 27-28 April 2019	Shailendra Singh, Girish Wadhwa and Balwinder Raj, Analysis of Scalable Si-Ge layer embedded in Channel of Vertical Tunnel FET for Low Power Digital Applications,
2019	CPIE 2019, NIT Jalandhar, 08-10 June 2019	Shailendra Singh, Girish Wadhwa and Balwinder Raj, "Analysis of Ion and Ambipolar Current for Scalable Embedded SiGe-Junction in Vertical-Channel TFET",
2018	15-17 Dec, ICSCCC-2018, CSE, NIT Jalandhar	Shailendra Singh, Balwinder Raj, "Vertical Tunnel FET Analysis for Excessive Low Power Digital Applications",
2018	Ghaziabad, India on 21-22 July	Neeraj Jain and Balwinder Raj, "Capacitance/Resistance Modeling and Analog Performance Evaluation of 3-D SOI FinFET Structure for Circuit Perspective Applications" 2nd International conference on Frontiers of Science & Technology(ICFST-18)
2018	ICCCN 2018, National Institute of Technical Teachers Training and Research, Chandigarh, India, March 29-30, 2018	Gurmohan Singh, R. K. Sarin and Balwinder Raj, "Reliability Aware Design and Performance Analysis of QCA Based Exclusive-OR Gate"
2017	(RISE-2017) 27-29 October	Bharat Tripathi, Saurabh Khandelwal, Ravi Shrivastava, Balwinder Raj "Implementation of Leakage Reduction Techniques in FinFET based 3T DRAM based at 45 nm Technology
2017	ICET: EITM-2017), NIT Hamirpur, Dec, 2017.	Jeetendra Singh, and Balwinder Raj, "Simulation and performance analysis of Ideal memristor Model with Various Window Function to investigate Memristive SRAM Cell"
2016	(IEEE-GCCE 2016), Kyoto, Japan from 11th to 14th Oct 2016	Amandeep Singh, Mamta Khosla, Balwinder Raj "CNTFET Modeling and Low Power SRAM Cell Design"
2016	International Conference on Electrical Electronics and Industrial Automation, Pattaya, Thailand, from 23rd to 24th Jan 2016	Sunil Kumar and Balwinder Raj, "Simulation of Nanoscale TFET Device Structure for Low Power Applications"

2015	(IEEE-GCCE 2015), Osaka, Japan from 27th to 30th Oct 2015	Sanjeev Kumar Sharma, Mamta Khosla, Balwinder Raj, “Performance Enhancement of Junctionless Nanowire FET with Laterally Graded Channel Doping and High-? Spacers” in IEEE Global Conference on Consumer Electronics
2015	(IEEE-GCCE 2015), Osaka, Japan from 27th to 30th Oct 2015	Amandeep Singh, Mamta Khosla, Balwinder Raj “Comparative Analysis of Carbon Nanotube Field Effect Transistors”
2015	IEEE Computer Society, JIIT, Noida, India, 20-22 Aug 2015	Sunil Kumar and Balwinder Raj, “Modeling of DG-Tunnel FET for Low Power VLSI Circuit Design,” 2015 Eighth International Conference on Contemporary Computing (IC3), IC3-2015 - Systems (Hardware & Software),
2014	Centre for Nano Science and Engineering, IISC Banglore, held on 22-23 August-2014	Sunil Kumar and Balwinder Raj, “Compact channel potential analytical Modeling of DG-TFET based on Evanescent–mode Approach,” INUP Familiarization on compact Modeling workshop,
2014	Poster presentation in Industry-Academia Conclave at IIT Indore, 11-12 September, 2014	Amandeep Singh, Mamta Khosla, Balwinder Raj “CNTFET for Industrial Applications”
2013	(CACCS 2013) DIT Dehradun, India, 6-8th Apl 2013	Balwinder Raj, “Noise Margin and Delay Analysis of Half Stacked and Full Stacked SRAM Cell Design
2013	(ICETET 2013), IT Society of India, New Delhi, India Apr 14, 2013	Maisagalla Gopal and Balwinder Raj, “Low Power 8T SRAM cell Design for High Stability Video Applications”, International Conference on Emerging Trends in Engineering and Technologies
2012	(NanoSciTech 2012), Punjab University Chandigarh, February 16-18, 2012	Balwinder Raj, “A Quantum Mechanical Potential Analysis of FinFET Device through Quantum Inversion Charge: Modeling and Simulation Approach”,
2012	(ICECT 2012), Kanyakumari, India, April 6 - 8, 2012	Shashikant Sharma, Anjan Kumar, Manisha Pattanaik and Balwinder Raj, “Forward Body Biased Multimode Multi-Threshold CMOS Technique for Ground Bounce Noise Reduction in Static CMOS Adders”
2012	IEEE International Symposium on Electronic System Design (ISED), Kolkata pp. 272-275, 2012	Shashikant Sharma, C. Periasamy, Manisha Pattanaik and Balwinder Raj, “Signal Stepping Based Multimode Multi-Threshold CMOS Technique for Ground Bounce Noise Reduction in Static CMOS Adders”,
2012	International Conference on Nanomaterials and Electronics Engineering, July 24-26, 2012 Kuala Lumpur, Malaysia	H. S. Jatav, Balwinder Raj and P. Srivastava, “Performance Analysis of Threshold Logic Gate Single-Electron Transistor Full Adder,” Elsevier,
2012	IEEE 3rd International Conference on Computing Communication And Networking Technologies, Trichy, India, 2012	Shashikant Sharma, Anjan Kumar, Manisha Pattanaik and Balwinder Raj” Ground Bounce Noise Reduction using Ultra Low Power Diode Based Multi-Threshold CMOS Technique for Static CMOS Adder,”
2011	(SocProS 2011), IIT Roorkee, Dec 20-22, 2011	Balwinder Raj, A. K. Saxena and S. Dasgupta , “Quantum Mechanical Analytical Drain Current Modeling and Simulation for Double Gate FinFET Device using Quasi Fermi Potential Approach,” International Conference on Soft Computing for Problem Solving

Book/Chapter Publications :

Type	Title	Publisher	Authors	ISBN/ISSN No.	Year
Book Chapter	Nanoscale Memristor Device for Analog and Digital Application	CRC Press, PP. 393-423, 2018	Jeetendra Singh and Balwinder Raj	9781138060340	2018
Book Chapter	Analysis of Dynamic Linear Memristor Device Models, Book: Advances in Memristors, Memristive Devices and Systems,	Springer	Balwinder Raj	978-3-319-51723-0	2017
Book Chapter	Simulations and Modeling of TFET for Low Power Design	IGI Global, USA	Sunil Kumar and Balwinder Raj		2015
Book Chapter	Quantum Mechanical Potential Modeling of FinFET	Springer	Balwinder Raj	978-3-319-02021-1	2014
Book	VLSI Design and Fabrications	University Science Press	Balwinder Raj, B. Singh and Ashish Dixit	978-93-81159-60-6	2013
Book Chapter	SRAM Cells for Embedded Systems	InTech Europe	Jawar Singh and Balwinder Raj	ISBN 979-953-307-580-7	2012

Research Projects :

Role	Project Type	Title	Funding Agency	From	To	Amount	Status	Co-Investigator
Coordinator	Research Infrastructure Development	Characterization of Nanoscale Semiconductor Devices	DST-FIST	2014	2019	165 Lakhs	Ongoing	Dr. Arun Khsola, Dr. Mamta Khosla and Dr. Balwinder Raj
PI	Research Project	Compact Quantum Mechanical Mobility Model for Surrounding Gate Transistor: Modeling and TCAD Simulation Approach	DIT Under INUP IIT Bombay	2012	2014	6 Lakhs	Completed	
PI	Research under Exchange Program	Aalto-IITI cooperation for the skill developments of IoT based implementation	CIMO Asia programme jointly with Aalto University, Finland and IIT Indore, India	2016	2018	40000 Euro's	Completed	Dr. S K Vishvakarma

PI	Research Project	Design and Development of Low Power ONOFIC for Smart Safety System	SERB-DST	2017	2020	47 Lakhs	Ongoing	--
PI	Research Project	Design and Development of Junctionless Nanowire TFET Biosensor	SERB-DST	2019	2022	37 Lakhs	Ongoing	--

Events Organized :

Category	Type	Title	Venue	From	To	Designation
Conference-Special Session on “Microelectronics and VLSI Design”	International	IEEE 4th Global Conference on Consumer Electronics (GCCE-2015)	Osaka International Convention Center, Japan on October 27-30, 2015.	27-10-2015	30-10-2015	Session Chair
Conference--• Special Session on “Bio-Inspired VLSI and Embedded System Design”	International	Seventh International Conference on Bio-Inspired Computations: Theory and Applications (BICTA 2012),	ABV-IIITM Gwalior	14-12-2012	16-12-2012	Session Chair
Self Financed Short Term Course	National	Electronics and Communication Systems Design Aspects	VLSI Design Lab, ECE, NIT Jalandhar	25-05-2015	29-05-2015	Coordinator
One-week Industrial-Institute-Interaction training program sponsored by TEQIP-II	National	Emerging Trends of Research in Electronics and Communication	VLSI Design Lab,ECE, NIT Jalandhar	01-12-2014	05-12-2014	Chief Coordinator

Training program	International	10 days training program on “Research-Teaching Exchange Excursion Workshop” jointly organized by Dept. of ECE, NIT Jalandhar and Techical University of Munich, Germany,	VLSI Design Lab, ECE Dept. NIT Jalandhar	15-09-2016	24-09-2016	Coordinator
One-week Self Financed Short Term Course	National	“Research Trends in VLSI Devices and Circuits Co-design” held from 4th to 8th May-2018	VLSI Design Lab, NIT Jalandhar	04-05-2018	08-05-2018	Coordinator
One Week STC under TEQIP-III	National	Current avenues of research in Electronics & Communication Engineering" jointly with GWEC Ajmer	NKN Hall IT Park NIT Jalandhar	25-03-2019	29-03-2019	Coordinator

Professional Affiliations :

Designation	Organization
Life member (Membership No. L-1234).	Punjab Academy of Sciences, Patiala, India
Life Member (Membership No. LM-93041)	Indian Society for Technical Education (ISTE)”, IIT(Delhi) Campus, Katwaria Sarai, New Delhi
Life member, (Membership No. M-231963).	Institution of Electronics and Telecommunication Engineers (IETE), New Delhi, India
Member (Membership No. M-159543-6)	Institution of Engineers, Kolkata, India
Member (Membership No. 94127067).	IEEE & Electron Devices Society (EDS), USA

PhD Supervised :

Scholar Name	Research Topic	Status	Year	Co-Supervisor
Mr Jeetendra Singh	MODELING AND SIMULATION OF MEMRISTOR FOR MEMORY CELL DESIGN	Thesis Submitted	2019	--
Mr. Neeraj Jain Ph.D (Reg. No. 13804003)	Nano Scale FinFET Modeling and Simulation for Analog Circuit Design	Completed	2018	--
Mr. Gurmohan Singh (Reg. No. 14804001)	Design and Performance Analysis of Quantum Cellular Automata Based Nanocomputing Circuits	Completed	2018	Dr. R K Sarin
Mr. Sunil Kumar (Reg. No. 12404004)	Design and Analysis of Tunnel FET Device for Low Power SRAM Cell	Completed	2017	--
Mr. Amandeep Singh Rehal (Reg. No. 13504002)	Modeling and Simulation of Carbon Nanotube FET for Ultra Low Power SRAM Design	Completed	2017	Dr. Mamta Khosla

Mr. Sanjeev Kumar Sharma (Reg. No. 13504006)	Analysis of Nanowire FET and its Application as Low Power Sensor Design	Completed	2017	Dr. Mamta Khosla

Award and Honours :

Title	Activity	Given by	Year
Early Carrier Research Award	Research work on TFET and and its Applications	SERB-Department of Science and Technology, New Delhi, India	2017
Young Scientist Award	18th Punjab Science Congress	Punjab Academy of Sciences, Punjabi University Patiala, Punjab, India	2015
Best Paper Award	International Conference on Electrical and Electronics Engineering on 11-12 July 2015	IRP, Pattaya, Thailand	2015
Best Teacher Award	43rd ISTE Section Convention	Indian Society for Technical Education (ISTE) New Delhi	2013