Inauguration of

Short Term Course on "**Low Power VLSI Design for Communication Systems and Networks**"

On 16-09-2020 at 11:30 AM-12:00 Noon

Organized by Department of Electronics and Communication Engineering from 16th to 20th September 2020

Dr B R Ambedkar National Institute of Technology, Jalandhar

STC Organizers:

1. Dr Manjeet Singh - Coordinator
2. Dr Tarun Chaudhary-Coordinator
3. Dr Ramesh K Sunkaria-Convener

Power dissipation has become an important consideration as performance and area for VLSI Chip design. With shrinking technology reducing power consumption and over all power management on chip are the key challenges below 100nm due to increased complexity. For many designs, optimization of power is important as timing due to the need to reduce package cost and extended battery life. The low power design for communication systems are in real demand for green information and communication technologies (ICT). It is observed that more than 35% of total power consumption in the world is utilized by ICT devices. In this concern, saving of ICT devices power is now becoming a social responsibility. power has emerged as a principal theme in today's world of electronics industries.