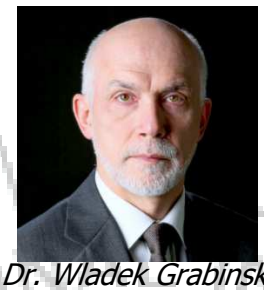
Dr. B.R. Ambedkar National Institute of Technology, Jalandhar, Punjab
Department of Electronics and Communications Engineering

Webinar

FOSS TCAD/EDA Tools for Semiconductor Device Modeling

Date: 18th September 2020, Time [3:30 pm to 05:00 pm]



Dr. Wladek Grabinski
Senior Member-IEEE MOS-AK Association (EU)

Abstract: Compact/SPICE models of circuit elements (passive, active, MEMS, RF) are essential to enable advanced IC design using nanoscaled semiconductor technologies. Compact/SPICE models are also a communication means between the semiconductor foundries and the IC design teams to share and exchange all engineering and design information. To explore all related interactions, we are discussing selected FOSS CAD tools along complete technology/design tool chain from nanascaled technology processes; thru the compact modeling with EKV and EKV-HV examples; to advanced IC transistor-level design support. New technology and device development will be illustrated by application examples of the FOSS TCAD tools: Cogenda TCAD and DEVSIM. Compact modelingwill be highlighted by review topics related to its parameter extraction and standardization of the experimental and measurement data exchange formats. Finally, we will present two FOSS CAD simulation and design tools: ngspice and Qucs. Application and use of these tools for advanced IC design (e.g. analog/RF IC applications) directly depends on the quality of the compact model implementations in these tools as well as the reliability of extracted models and generated libraries/PDKs. Discussing new model implementation into the FOSS CAD tools (Gnucap, Xyce, ngspice and Qucs as well as others) we will also address an open question of the compact/SPICE model Verilog-A standardization. We hope that this presentation will be useful to all the researchers and engineers actively involved in the developing compact/SPICE models as well as designing the integrated circuits in particular at the transistor level and then trigger further discussion on the compact/SPICE model Verilog-A standardization and development supporting FOSS CAD tools.

WladekGrabinski received the Ph.D. degree from the Institute of Electron Technology, Warsaw, Poland, in 1991. From 1991 to 1998 he was a Research Assistant at the Integrated Systems Lab, ETH Zürich, Switzerland, supporting the CMOS and BiCMOS technology developments by electrical characterization of the processes and devices. From 1999 to 2000, he was with LEG, EPF Lausanne, and was engaged in the compact MOSFET model developments supporting numerical device simulation and parameter extraction. Later, he was a technical staff engineer at Motorola, and subsequently at Freescale Semiconductor, Geneva ModelingCenter, Switzerland. He is now a consultant responsible for modeling, characterization and parameter extraction of MOS transistors for the design of RF CMOS circuits. He is currently consulting on the development of next-generation compact models for the nanoscaled technology very large scale integration (VLSI) circuit simulation. Wladek is a member ESSDERC TPC Track4: "Device and circuit compact modeling" as well as is serving as a member of the IEEE EDS Compact Modeling Technical Committee, organization committee of ESSDERC/ESSDERC, TPC of SBMicro, SISPAD, MIXDES Conferences; reviewer of the IEEE TED, IEEE MWCL, IJNM, MEE, MEJ. He also continued as a European representative to the ITRS Modeling and Simulation working group. He was a Member At Large of Swiss IEEE ExComand mentored the EPFL IEEE Student Branch acting as its Interim Branch Counselor. Wladek is involved in activities of the MOS-AK Association and serves as a coordinating manager since 1999.

Link: https://bit.ly/3iytNNq

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