Expt No. I.

RESISTIVITY DETERMINATION FOR A SEMICONDUCTOR WAFER USING FOUR PROBE METHOD

APPARATUS:

Probes Arrangement, Sample, Power supply, Oven etc.

THEORY:

The properties of the materials used for the fabrication of semiconductor devices, like transistors etc., are essential in determining the characteristics of the devices. Resistivity measurements are generally made on semiconductors, like germanium and silicon, to determine their suitability. The Resistivity must be measured accurately since its value is critical in many devices.

(i) ELECTRONIC CONDUCTION IN SOLIDS:

The electrical properties of semiconductors involve the motion of charged particles within them. Therefore, we must have an understanding of the forces which control the motion of these particles. It is of course, the physical structure of the solid which exerts their control.

Atoms, of which a solid is composed, consist of positively charged nuclei with electron orbiting around them. Negatively charged electrons compensate the positive charge, so that a complete atom is electrically neutral. Electrons are arranged in shells, and the closer they are to the nucleus the more strongly they are bound. If we take the particular case of silicon, a well known semiconductor, we find that it has fourteen electrons which are accommodated in the shells as $(1S)^2$, $(2S)^2$, $(2P)^6$, $(3S)^2$, $(3P)^2$. Since the third shell is not even half filled, the four electrons are available for chemical binding giving silicon a valency of four. (Germanium also has a chemical valency of four, but from the fourth shell).

Let us now concentrate our attention on solids, If we bring many atoms close to one another, interatomic forces become quite strong as electronic orbits begin to overlap. The outershell electrons play an important role, because their orbits are the most disturbed. These electrons are no longer associated with a particular atom, the outer shell electron may make an orbit around one atom and continue about another. In this fashion, the outer shell or valency electrons are continually traded among atoms and wander all over the solid. The continuous interchange of valence electrons between atom holds the solid together. This is the predominant type of bonding in silicon and germanium, and is called the valence bonding.

In solids, atoms are usually arranged in a regular way to achieve dense packing and thereby form a crystal. The arrangement has very desirable characteristics, i.e. the transport of holes and free electrons is very smooth in these structures. When the arrangement is not crystalline, complication arises. Here we will be concerned only with the properties of perfect crystals. Silicon and germanium (and carbon) crystallize with an identical crystal structure, the so called diamond structure.

Figure 1 shows a potential diagram of an array of atoms. An actual crystal is of course three-dimensional. The most important difference between the potential plot of an isolated atom and one-dimensional array is the splitting of energy levels. In fact, bringing N atoms together we find 'N' times as many levels throughout the crystal.

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The spreading of energy level depends on the degree of interaction, therefore, the inner orbits split into levels combined in a narrow energy than the outer ones.

As a result of the interaction between the tremendous number of atoms in crystal (10^{22} per cm^3), the energy level found in isolated atoms will be split and form bands of allowed energies which contain almost continuum of levels. Accordingly, electrons are located in energy bands in crystalline solid. The band, which contains the valence electrons, is called the valence band. The unoccupied energy levels also split and form another band called the conduction band. The interaction between the unused shells is very large and they spread widely. Therefore, while there is a bandgap, E_g (or forbidden region) between the valence and conduction bands, splitting of higher orbit is so wide that they usually overlap.

The bands below the energy gap E_g are completely filled at absolute zero temperature and the conduction band is empty. This is a very important point and has direct consequences on the conduction properties. The fundamental theory is that current conduction is not possible in empty and filled bands. The reasons about the empty band is obvious since current is not possible without carriers. On the other hand in the filled band, though the valence electrons move about the crystal but they can not be accelerated because the acceleration means gain of energy and there are no higher energy levels available to which they could rise.

We can now readily see that the crystal band structure shown in Figure 1 does not allow current conduction at T=0. If we increase the temperature, however, thermal agitation increases and some valance electron will gain energy greater than E_g and jump into the conduction band. The electron in the conduction band is called free electron, and its former place in the valance band is called a hole. Electrons in conduction band can gain energy when a field is applied, because there are many higher energy states available. The fact that electrons left the valance bands leaves some empty energy levels, this allows conduction in the valance band as well. Electrons can now gain energy in the valance band also, and we observe motion of holes in the direction of the field. Because of this, we begin to speak of a hole as a current carrying particles.

As per foregoing discussions, an insulator must have large band gap. So that at room temperature the conduction band is practically, empty. The valance band is practically filled. The semiconductors must have a narrow band gaps so that appreciable number of carriers are present in the valance and conduction bands at room temperature..

In metals, however, the valance and conduction bands overlap and application of an electric field can therefore, accelerate many electrons. The non-existences of a band gap make conduction in metal almost independent of temperature, as compared to semiconductors. Figure 2 summarizes the above points.

The fact that electrons can be found in energy bands within a crystal and other conclusions mentioned so far can be shown by quantum mechanical calculations. Which shall not carry out here, but the results are used for quantitative analysis.

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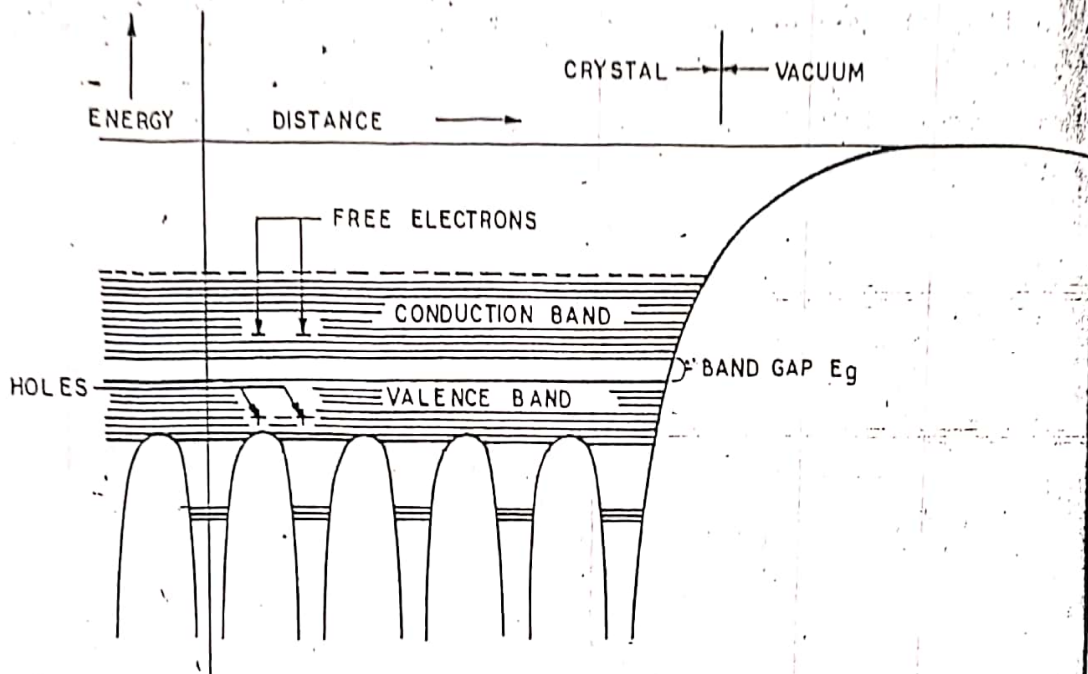

FIG. 1 UNUSED SHELLS FORM THE CONDUCTION BAND

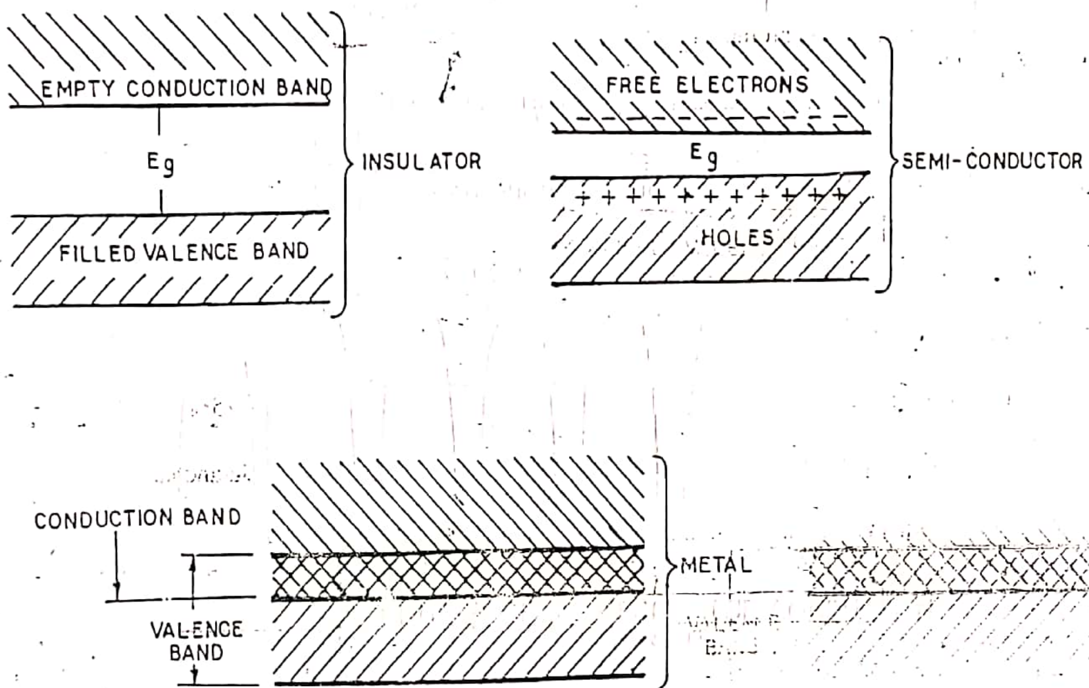

FIG. 2 BAND STRUCTURES FOR INSULATORS, SEMICONDUCTOR AND METALS

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Concentration of Intrinsic carriers:

The concentration of intrinsic carrier (the number of electrons in conduction band per unit volume) is given by expression:

$$n = 2\left(\frac{m_e.\ k.\ T}{2\pi\ h^2}\right)^{3/2} \text{Exp}\ (\mu - E_g)\ /kT \qquad ....(1)$$

and the concentration of holes in valance band is given by the expression :

$$p = 2\left(\frac{m_h.\ k.\ T}{2\pi\ h^2}\right)^{3/2} \text{Exp}\ (-\ \mu\ /kT\ ) \qquad ....(2)$$

If we multiply together the expression for n and p to obtain equilibrium relation:

$$np = 4\left(\frac{k.\ T}{2\pi\ h^2}\right)^{3} (m_e\ m_h)^{3/2} \quad \text{Exp}\ (-\ E_g/kT\ ) \qquad ....(3)$$

This does not involve the fermi level μ and is known as the expression of law of mass action.

Where m_e = effective mass of an electron
m_h = effective mass of a hole
k = Boltzmann's constant
E_g = band gap μ
μ = fermi level
T = temperature in ^oK

In case of intrinsic (highly purified) crystals, the number of electrons is equal to the number of holes, because the thermal excitation of an electron leaves behind a hole in the valance band. Thus from (3) we have, letting the subscript i denote intrinsic

$$n_i = p_i = 2\left(\frac{k.\ T}{2\pi\ h^2}\right)^{3/2} (m_e\ m_h)^{3/4} \quad \text{Exp}\ (-\ E_g/2kT\ ) \qquad ....(4)$$

Thus, we see that the concentration of intrinsic carrier depend exponentially on $E_g/2kT$.

Conductivity of Intrinsic Semiconductor :

The electrical conductivity will be the some of the contributions of both electrons and holes:

$$\sigma = (n_i\ e\ \mu_e + p_i\ e\ \mu_h) \qquad ....(5)$$

Where e is the electron charge. μ_e and μ_h are the average velocities acquired by the electrons and holes in a unit electric field and are known as mobilities.

Or $\sigma = e\ n_i\ (\mu_e + \mu_h)$ since $n_i = p_i$

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Using Eq. 4

$$\sigma = (K)\, T^{3/2}\ (\mu_e + \mu_h).\ \mathrm{Exp}\,(-\,E_g/2kT) \qquad \ldots\ldots..(6)$$

Where K is a constant. The factor $T^{3/2}$ and the mobilities change relatively slow with temperature. The exponential term, and hence the logarithm of resistivity ρ (=1/σ) varies linearly with 1/T. The width of the energy gap may be determined from the slope of the curve.

Thus, we have,

$$\mathrm{Log}_e\, \rho = (E_g/2kT) - \log_e K \qquad \ldots\ldots..(7)$$

(ii) FOUR PROBE METHOD

Many conventional methods for resistivity measurements are unsatisfactory for semi-conductors because metal-semiconductor contacts are usually rectifying in nature. Also there is generally minority carrier injection by one of the current carrying contacts. An excess concentration of minority carriers will affect the potential of other contacts and modulate the resistance of the material.

The method described here overcomes the difficulties mentioned above and offers several other advantages. It permits measurements of resistivity in samples having a variety of shapes, including the resistivity of small volumes within bigger pieces of semiconductor. In this manner, the resistivity on both sides of a p-n junction can be determined with good accuracy before the material is cut into bars for making devices. This method of measurement is also applicable to silicon and other semiconductor materials.

The basic model for all these measurements is indicated in Figure 3. Four sharp probes are placed on a flat surface of the material to be measured, current is passed through the two outer electrodes, and the floating potential is measured across the inner pair. If the flat surface on which the probe rest is adequately large of a big crystal, the specimen may be considered a semi-infinite volume. To prevent minority carrier injection and make good contact, the surface on which the probes rest may be mechanically lapped.

The experimental circuit used for measurement is illustrated schematically in Figure 4. A nominal value of probe spacing, which has been found satisfactory, is an equal distance of 1.25 mm between adjacent probes. This permits measurement with reasonable currents of n – or p – type semiconductor.

In order to use this four-probe method in semiconductor crystals or slices it is necessary to assume that:

1. The resistivity of the material is uniform in the area of measurement.
2. If there is minority carrier injection into the semiconductor by the current-carrying electrodes most of the carriers recombine near the electrodes so that their effect on the conductivity is negligible. (This means that the measurements should be made on surfaces, which have a high recombination rate, such as mechanically lapped surfaces).
3. The surface on which the probes rest is flat with no surface leakage.

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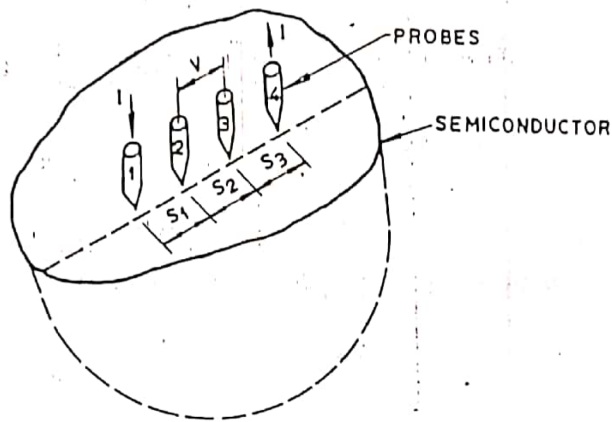

FIG. 3 MODEL FOR THE FOUR PROBE RESISTIVITY MEASUREMENTS

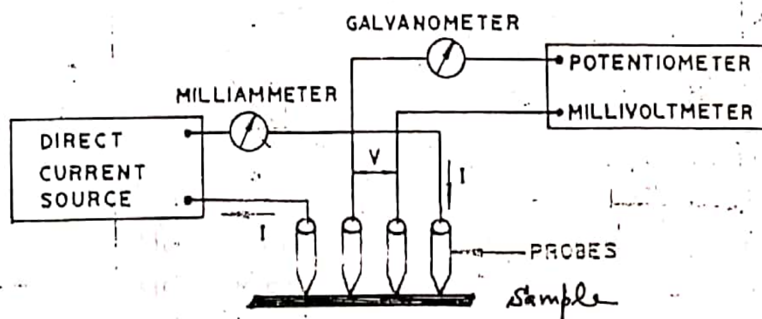

FIG. 4 CIRCUIT USED FOR RESISTIVITY MEASUREMENTS

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4. The four probes used for resistivity measurement contact the surface at points that lie in a straight line.
5. The diameter of the contact between the metallic probes and the semiconductor should be small compared to the distance between probes.
6. The boundary between the current-carrying electrodes and the bulk material is hemispherical and small in diameter.
7. The surface of the semiconductor crystal may be either conducting or non-conducting.
   (a) A conducting boundary is one on which a material of much lower resistivity than semiconductor (such as copper) has been plated.
   (b) A non-conducting boundary is produced when the surface of the crystal is in contact with an insulator.

Case 1: Resistivity Measurements on a Large Sample:
One added boundary condition is required to treat this case namely, that the probes are far from any of the other surfaces of the sample and the sample can thus be considered a semi-infinite volume of uniform resistivity material. Figure 3 shows the geometry of this case, Four probes are spaced S_1, S_2 and S_3 apart. Current I is passed through the outer probes (1 and 4) and the floating potential is measured across the inner pair of probes (2 and 3).

The floating potential V_f a distance r from an electrode carrying a current I in a material of resistivity ρ_o is given by

$$V_f = \frac{\rho_o I}{2\pi r}$$

In the model shown in Figure 3 there are two current-carrying electrodes, numbered 1 and 4, and the floating potential V_f at any point in the semiconductor is the difference between the potential induced by each of the electrodes, since they carry currents of equal magnitude but in opposite directions. Thus:

$$V_f = \frac{\rho_o I}{2\pi}\left(\frac{1}{R_1} - \frac{1}{R_4}\right) \qquad ....(9)$$

Where:

R_1 = distance from probe number 1.
R_4 = distance from probe number 4.

Let the floating potentials at probe 2 is V_{f2} and at probe 3 is V_{f3}, that can be calculated from (9) by substituting the proper distances as follows:

$$V_{f2} = \frac{\rho_o I}{2\pi}\left(\frac{1}{S_1} - \frac{1}{S_2 + S_3}\right)$$

$$V_{f3} = \frac{\rho_o I}{2\pi}\left(\frac{1}{S_1 + S_2} - \frac{1}{S_3}\right)$$

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The potential difference V between probes is then

$$V = V_{f2} - V_{f3} = \frac{\rho_o I}{2\pi}\left(\frac{1}{S_1} + \frac{1}{S_3} - \frac{1}{S_2 + S_3} - \frac{1}{S_1 + S_2}\right)$$

and the resistivity ρ is computable as

$$\rho_o = \frac{V}{I}\;\frac{2\pi}{\left(\frac{1}{S_1} + \frac{1}{S_3} - \frac{1}{S_1 + S_2} - \frac{1}{S_2 + S_3}\right)} \quad \text{....(10)}$$

When the point spacing is equal, that is $S_1 = S_2 = S_3 = S$, the above simplifies to

$$\rho_o = V/I \times 2\pi s \quad \text{....(11)}$$

Case 2: Resistivity Measurement on a Thin Slice-Conducting Bottom Surface.
Two boundary conditions must be met on this case; the top surface of the slice must be a reflecting (non-conducting) surface and the bottom surface must be an absorbing (conducting) surface. Since the two boundaries are parallel, a solution by the method of images requires for each current source. An infinite series of images along a line normal to the planes and passing through the current source.

The model for this case is shown in Figure 5. The side surface of the specimen is assumed to be far from the area of measurement and, therefore, only the effect of the bottom surface needs to be considered. In this analysis equal probe, spacing S shall be assumed. The width of the slice is W. The array of images needed is indicated in Figure 5. Where the polarity and spacing of the first few images are shown.

The floating potential V_{f2} at electrodes 2 is:

$$V_{f2} = \frac{\rho I}{2\pi}\left[\sum_{n=-\infty}^{n=\infty} (-1)^n \frac{1}{\sqrt{\{S^2 + (2nw)^2}} - \sum_{n=-\infty}^{n=\infty} (-1)^n \frac{1}{\sqrt{\{(2S)^2 + (2nw)^2}}\right] \quad \text{...(12)}$$

Likewise, the floating potential at electrode (3) can be obtained and

$$V = \frac{\rho I}{2\pi}\left[\frac{1}{S} + \sum_{n=1}^{n=\infty} (-1)^n \frac{4}{\sqrt{\{S^2 + (2nw)^2}} - \sum_{n=1}^{n=\infty} (-1)^n \frac{4}{\sqrt{\{(2S)^2 + (2nw)^2}}\right] \quad \text{...(13)}$$

The resistivity then becomes

$$\rho = \frac{\rho_o}{G_6\,(W/S)} \quad \text{...(14)}$$

Where resistivity ρ_o is computable from (10), and (11) can be used if the spacings are different, but approximately equal. The function G_6 (W/S) is computed from

$$G_6\,(W/S) = 1 + 4\frac{S}{W}\sum_{n=1}^{n=\infty} (-1)^n \left[\frac{1}{\sqrt{\{(S/W)^2 + (2n)^2\}}} - \frac{1}{\sqrt{\{(2S/W)^2 + (2n)^2\}}}\right]$$

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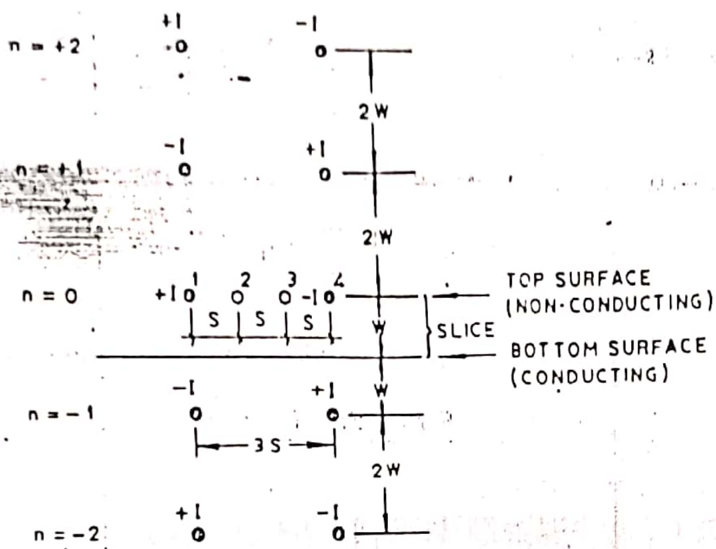

FIG. 5 IMAGES FOR THE CASE OF THE RESISTIVITY PROBES ON A THIN SLICE WITH A CONDUCTING BOTTOM SURFACE

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BRIEF DESCRIPTION OF THE APPARATUS REQUIRED:

1. **Probes Arrangements**: It has four individually spring loaded probes, coated with Zn at the tips. The probes are collinear and equally spaced. The Zn coating & individual spring ensure good electrical contacts with the sample. The probes are mounted in a Teflon bush which ensure a good electrical insulation between the probe. A Teflon spacer near the tips is also provided to keep the probes at equal distance. The whole arrangement is mounted on a suitable stand and leads are provided for current & voltage measurements.

2. **Sample:** Ge or Si crystal in the form of a chip.

3. **Oven:** It is a small oven for the variation of temperature of the crystal from room temperature to about 200°C.

4. **Four Probes Set-up**: (Measuring units) - It has three sub-units all enclosed in one cabinet.

(I) Multirange Digital Voltmeter

In this unit intersil 31/2 digit single chip A/D Converter ICL 7107 has been used. It has high accuracy, auto zero to less than 10 V, zero drift-less than 1 uV/°C, input bias current of 10 pA and roll over error of less than one cou... Since the use of internal r1eference causes the dgradation in performance due to internal heating, an external reference has been used.

(II) Constant Current Generator:

It is a IC regulated current generator to provide a constant current to the outer probes irrespective of the changing resistance of the sample due to change in temperatures.

The basic scheme is to use the feedback principle to limit the load current of the supply to a preset maximum value. Variations in the current are achieved by a potentiometer included for that purpose. The supply is a highly regulated and practically ripple free d.c. source. The current is measured by the digital panel meter.

(III) Over Power Supply:

Suitable voltage for the over in obtained through a step down transformer with a provision for low and high rates of heating. A glowing LED indicates, when the over Power supply is "ON".

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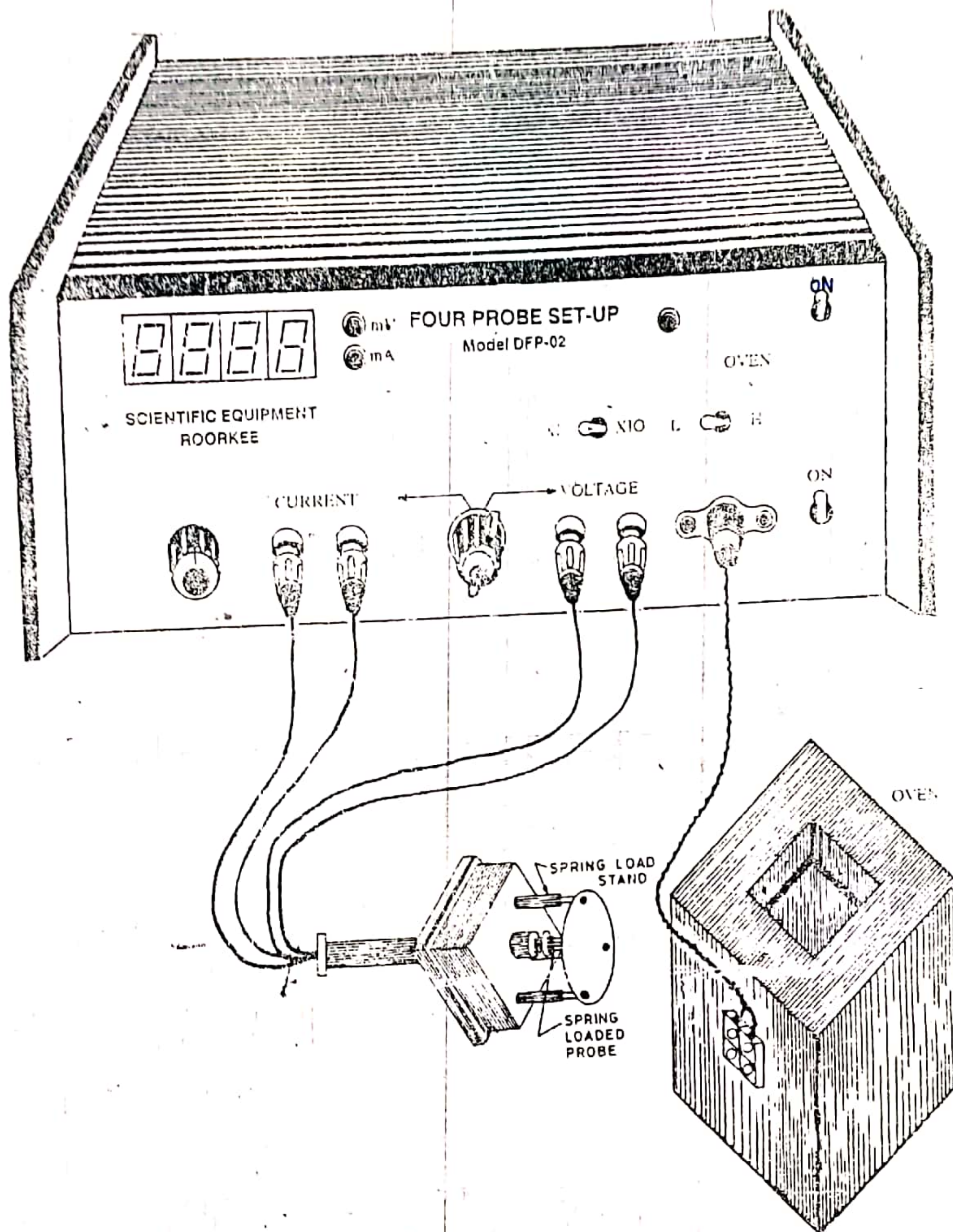

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s is tabulated in Table I.

TABLE I

/S	G_6 (W/S)	G_7(W/S)
00	0.0000019	13.863
41	0.00018	9.704
00	0.00342	6.931
33	0.0604	4.159
00	0.228	2.780
00	0.683	1.504
14	0.848	1.223
00	0.933	1.094
33	0.9838	1.0228
00	0.9948	1.0070
.00	0.9993	1.0045

se 3: Resistivity Measurements on a Thin Slice-Non-conducting Bottom Surface.
e model for these measurements is like for case 2, except that the bottom surface of slice is nonconducting. This means that all the images of Figure 5 have the same rge as the current source. Thus all the images on a row have equal charges and ation (13) describes the potential difference across the inner pair of probes if $(-1)^n$ removed from the equation. Then,

$$\rho = \frac{\rho_o}{G_7(W/S)} \qquad ...(16)$$

ere,

$$(W/S) = 1 + 4\frac{S}{W}\sum_{n=1}^{n=\infty}\left[\frac{1}{\sqrt{\{(S/W)^2 + (n)^2\}}} - \frac{1}{\sqrt{\{(2S/W)^2 + (2n)^2\}}}\right] \qquad (17)$$

is function G_7 (W/S) is tabulated in Table I. For smaller values of W/S the function (W/S) approaches the case for an infinitely thin slice, or

$$G_7\ (W/S) = \frac{2S}{W}\log_e 2. \qquad ....(18)$$

PERIMENTAL PROCEDURE :

Put the sample on the base plate of the four-probe arrangement. Unscrew the pipe holding the four probes and let the four probe rest in the middle of the sample. Apply a very gentle pressure on the probes and tighten the pipe in this position. Check the continuity between the probes for proper electrical contacts.

Caution:
The Ge crystal is very brittle. Therefore, use only the minimum pressure required for proper electrical contacts

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3. Place the four probe arrangement in the oven and fix the thermometer in the oven through the hole provided.

4. Switch on the Mains of Four probe set-up and put the digital panel meter in the current measuring mode through the selector switch. In this position LED facing mA would glow. Adjust the current to a desired value(Say 5 mA).

5. Now put the digital panel meter in voltage measuring mode, In this position LED facing mV would glow and the meter would read the voltage between the probes.

6. Connect the Oven Power Supply. Rate of heating may be selected with the help of a switch-Low or High as desired. Switch on the power to the Oven. The glowing LED indicates the power to the Oven is 'ON'

OBSERVATIONS & TABULATION

Current (I) = mA (Constant)

S. No.	Temperature °C	Voltage in volts	Temperature In °K	ρ Ohm.cm	(1/T) K° x 10^3	Log_{10} ρ

Distance between probes (s) = 2.0 mm

Thickness of the crystal (w) = ~~0.04 cm~~ 0.50 MM

CALCULATIONS :

Resistivity of the material ρ_o is given by

$$\rho_o = V/I \times 2\pi s$$

Since the thickness of the crystal is small as compared to the probe distances, a small correction factor for it has to be applied. Further the bottom surface is non-conducting in the present case,

$$\rho = \rho_o / G_7(w/s)$$

Where,

$$G_7(w/s) = 1 + 4(s/w) \sum_{n=0}^{n=\infty} \left[1/\{(s/w)^2 + (n)^2\}^{1/2} - 1/\{(2s/w)^2 + (2n)^2\}^{1/2} \right]$$

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The function G_7 (w/s) may be obtained from above expression for the appropriate value of (w/s). For smaller values of w/s the function $G_7(w/s)$ approaches the case for an infinitely thin slice, or

$$G_7(w/s) = 2(s/w) \log_e 2$$

Thus ρ may be calculated for various temperatures.

Plot a graph for $\log_{10} \rho$ vs 1000/T

Using following Eq

$$\log_e \rho = E_g/2KT - \log_e K$$

The slope of the curve is given by

$$\log_e \rho / (1/T) = E_g/2K$$

Thus E_g may be obtained from the slope of the graph. Note that $\log_e \rho = 2.3026 \log_{10} \rho$ and the above equation is applicable only in the intrinsic region of the semiconductor. A typical graph is shown in Figure 6.

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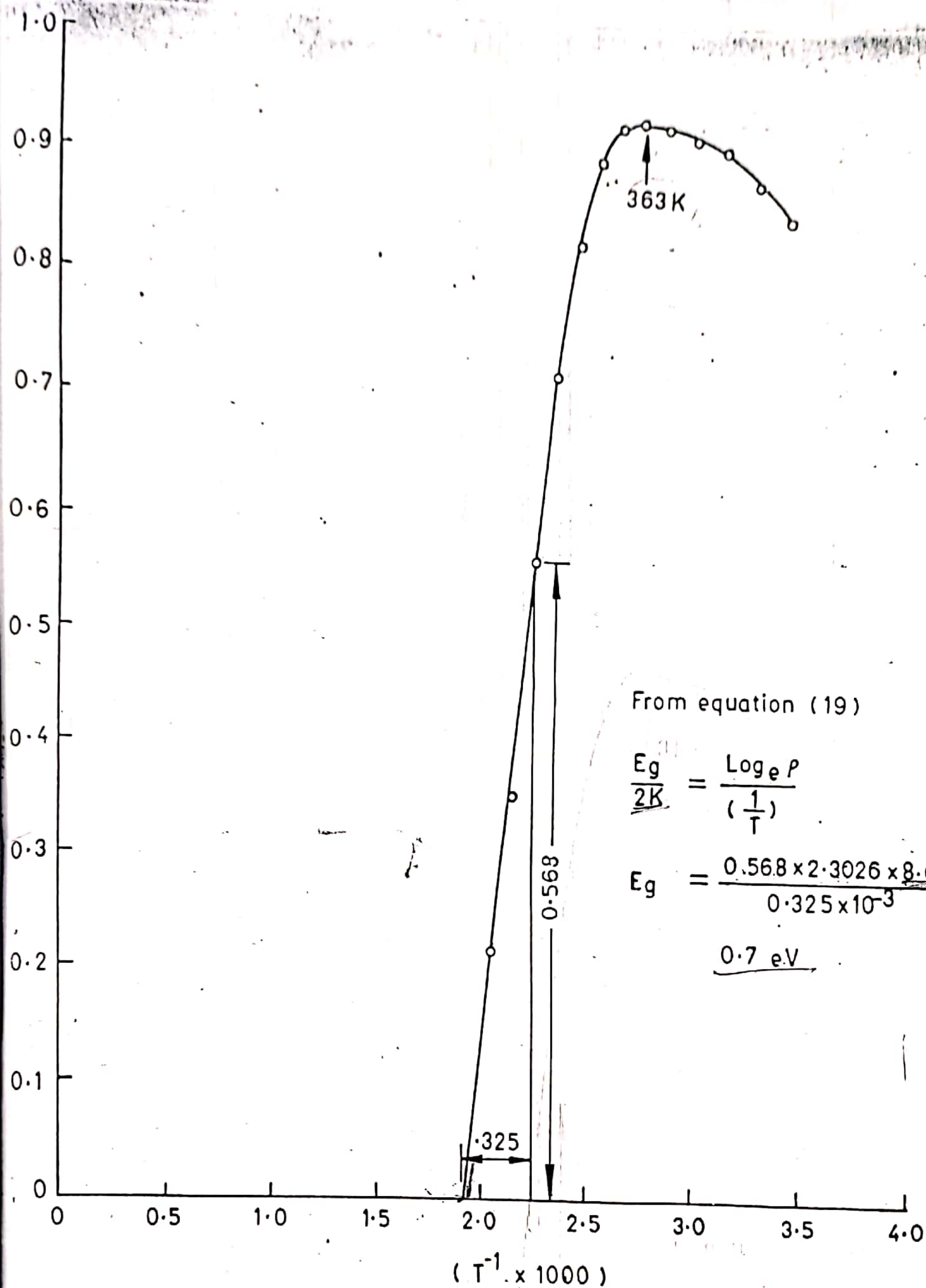

FIG. 6 THE RESISTIVITY OF A GERMANIUM CRYSTAL AS A FUNCTION OF INVERSE TEMPERATURE. FOR THIS SAMPLE $T < 363^{\circ}K$, CONDUCTION IS DUE MAINLY TO THE IMPURITY CARRIERS (EXTRINSIC REGION), FOR $T > 363$, CONDUCTION IS DUE TO ELECTRONS TRANSFERRED TO THE CONDUCTION BAND (AND THE CORRESPONDING HOLES CREATED IN THE VALENCE BAND). THIS IS THE INTRINSIC REGION.

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